IN THE CLAIMS

Please cancel claims 2-7, and 10, and amend claims 1, 9, and 11 as follows:

1. (Currently Amended) A storage device comprising:

a memory array including a plurality of memory blocks, each of which includes plural lines of cells ~~each including a plurality of cells~~ in correspondence with a data length;

a first register for storing a first address representing a first cell within a region ~~a start point~~ for storing a specific number of ~~first~~ data each having a same value;

an adder for adding run-length data representing the specific number of the ~~first~~ data each having the same value ~~consecutively repeated~~ to the first address so as to produce a second address;

a second register for storing the second address; [[and]]

a counter for supplying a write address designating a cell of the memory array subjected to a write operation;

a multiplexer for outputting the write address supplied from the counter to the memory array when performing the write operation and for outputting a read address to the memory array when performing a read operation; and

a controller for selecting a certain ~~controlling a~~ number of the cells within a line designated by the write address ~~in the plurality of memory blocks to be selectively and simultaneously placed in a write-enable state~~ based on the first address and the second address within the memory array to be simultaneously placed in a write-enable state,

wherein, when the region for storing the specific number of data, which are specified by the first address and the second address, lies in two or more lines of the cells, the counter increases the write address from a first write address to a second write address during execution of the write operation for writing the data into the region, the controller changes the cells, which

are simultaneously placed in the write-enable state, from a first number of cells designated by the first write address within a first line to a second number of cells designated by the second write address within a second line.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Previously Presented) A storage device according to claim 1, wherein the first data are pixel data produced by run-length coding on serial data.

9. (Currently Amended) A method for controlling a storage device that includes a plurality of memory blocks, each of which includes plural lines of cells ~~each including a plurality of cells~~ in correspondence with a data length, said method comprising:

storing a first address representing a first cell within a region ~~start point~~ for storing a specific number of ~~first~~ data each having a same value;

adding run-length data representing the specific number of the ~~first~~ data each having the same value ~~consecutively repeated~~ to the first address so as to produce a second address;

storing the second address; [[and]]

supplying a write address designating a cell of the memory array subjected to a write operation;

outputting the write address supplied from a counter to the memory array when performing the write operation and for outputting a read address to the memory array when

performing a read operation; and

selecting a certain ~~controlling a~~ number of the cells within a line designated by the write address ~~in the plurality of memory blocks to be selectively and simultaneously placed in a write-enable state~~ based on the first address and the second address within the memory array to be simultaneously placed in a write-enable state,

wherein, when the region for storing the specific number of data, which are specified by the first address and the second address, lies in two or more lines of the cells, the counter increases the write address from a first write address to a second write address during execution of the write operation for writing the data into the region, the controller changes the cells, which are simultaneously placed in the write-enable state, from a first number of cells designated by the first write address within a first line to a second number of cells designated by the second write address within a second line.

10. (Canceled)

11. (Currently Amended) A computer-readable medium having encoded thereon instructions which when executed implement a method for controlling a storage device that includes a plurality of memory blocks, each of which includes plural lines of cells ~~each including a plurality of cells~~ in correspondence with a data length, said method comprising:

storing a first address representing a first cell within a region ~~a start point~~ for storing a specific number of ~~first~~ data each having a same value;

adding run-length data representing the specific number of the ~~first~~ data each having the same value ~~consecutively repeated~~ to the first address so as to produce a second address;

storing the second address; [[and]]

supplying a write address designating a cell of the memory array subjected to a write

operation;

outputting the write address supplied from a counter to the memory array when performing the write operation and for outputting a read address to the memory array when performing a read operation; and

selecting a certain ~~controlling a~~ number of the cells within a line designated by the write address ~~in the plurality of memory blocks to be selectively and simultaneously placed in a write-enable state~~ based on the first address and the second address within the memory array to be simultaneously placed in a write-enable state,

wherein, when the region for storing the specific number of data, which are specified by the first address and the second address, lies in two or more lines of the cells, the counter increases the write address from a first write address to a second write address during execution of the write operation for writing the data into the region, the controller changes the cells, which are simultaneously placed in the write-enable state, from a first number of cells designated by the first write address within a first line to a second number of cells designated by the second write address within a second line.

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